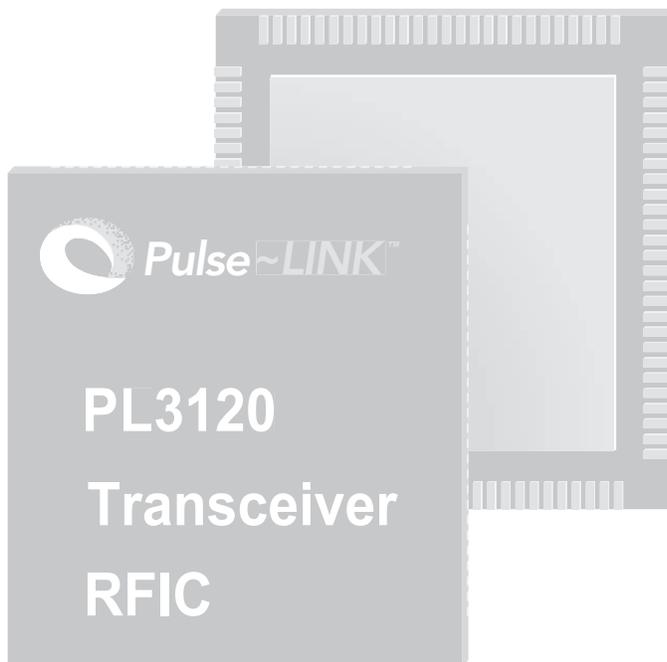


PL3120

**CWave[®]
Ultra
Wideband
Transceiver**





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CONTENTS

Introduction	1
Transmitter Block	2
Receiver Block	2
Control and Clock Reference Interfaces	2
Functional Descriptions	4
Transmitter Block	4
Receiver Block	4
Control Interfaces	5
Device Connections	7
Pad Configuration	7
Signal Description Summary	8
Electrical Specifications	15
Absolute Maximum Ratings	15
Recommended Operating Conditions	15
DC Characteristics	16
AC Electrical Characteristics	18
Typical Operating Circuit	22
Typical Operating Characteristics	23
Mechanical Specifications	23
Acronyms & Abbreviations	25
Ordering & Contact Information	26

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PL3120 CWave® Ultra Wideband Transceiver

Introduction

The PL3120 CWave® Ultra-Wideband Transceiver RFIC is an integral part of Pulse~LINK's CWave UWB chipset solution for high-speed wireless, coax cable, and hybrid connectivity. The PL3120 supports data rates up to 675 Mbps, and directly interfaces with the PL3130 Baseband+MAC, the PL3110 Low Noise Amplifier (LNA) for wireless applications and the PL3111 Analog Front End (AFE) for coax applications.

The PL3120 Ultra-Wideband Transceiver RFIC is an implementation of the CWave Biphase Shift Keying (BPSK) transceiver. This transceiver architecture provides a fully integrated receive path, transmit path, Voltage Controlled Oscillators (VCO), PLL frequency synthesis, and Baseband signal interfaces. The design is very robust and provides excellent noise immunity to substrate and power supply noise.

The transmitter block serializes data from the PL3130 Baseband+MAC chip, generates the 4 GHz carrier, and modulates the carrier with the high-speed data. The modulated signal then drives a gain-controlled differential power amplifier. The receiver block receives pre-amplified RF data from the PL3110 LNA, amplifies the signal, then over-samples it with a high-speed Analog-to-Digital Converter (ADC). The resulting digital data stream is next de-multiplexed. The chipset functional interface diagram in Figure 1 shows the PL3120 Transceiver RFIC as it fits into the high-performance Pulse~LINK CWave UWB chipset solution.

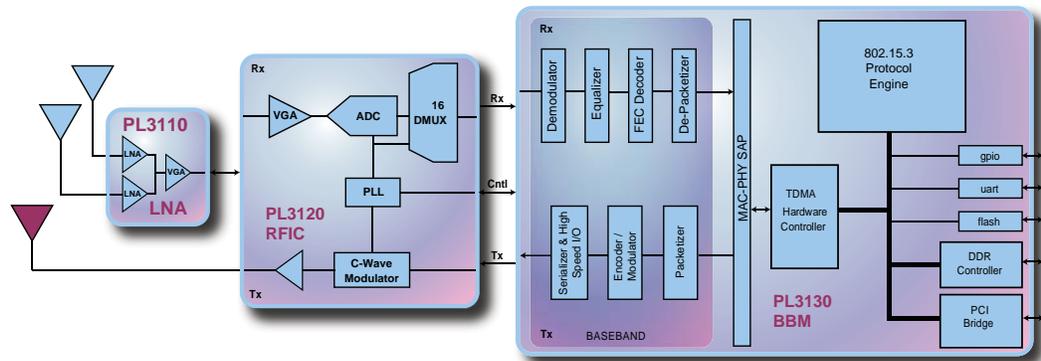


Figure 1: PL3120 Transceiver RFIC Functional Chipset Interfaces

Transmitter Block

The transmitter block of the PL3120 Transceiver RFIC is comprised of a CWave[®] BPSK modulator, gain-controlled differential Power Amplifier (PA), an 8.1 GHz Phase Lock Loop (PLL), and data/control signal input buffers. Main features of the PL3120 Transmitter Block:

- Dual 675 Mbps differential input Tx data streams
- 1.35 GHz CWave[™] UWB RF modulator
- 8.1 GHz PLL and VCO with 675 MHz external clock reference
- PA with 3-bit DAC output power control
- Direct interface with the PL3130 Baseband+MAC chip

Receiver Block

The receiver block of the PL3120 Transceiver RFIC contains a complete direct conversion receive path utilizing an over-sampling high-speed ADC and a 16-channel Demultiplexer. It provides fully integrated RF PLL/VCOs and enables use of an optional external clock source. Main features of the PL3120 Receiver Block:

- Three-stage VGA at receiver front-end
- 6-bit DAC controls receive VGA gain
- DAC for offset control
- 16 parallel differential outputs with 675 Mbps data rates
- Direct Interface with PL3130 Baseband+MAC chip and PL3110 LNA

Control and Clock Reference Interfaces

The PL3120 data and control interfaces consist of a Serial Peripheral Interface (SPI) bus, an external 675 MHz transmit clock reference, transmit clock control, and external RX, TX and RFIC enables. Main features of the RFIC Control and Reference Interfaces:

- SPI control interface
 - Transmitter PA power control
 - Receiver VGA gain control

- ADC offset control
- Various control and enable functions
- Digital TX/RX/Standby/Sleep Mode control
- External reference clock inputs for TX and RX
- Interfaces directly with the PL3130 Baseband+MAC chip

Functional Descriptions

A detailed functional block diagram of the PL3120 Transceiver RFIC is provided in Figure 3.

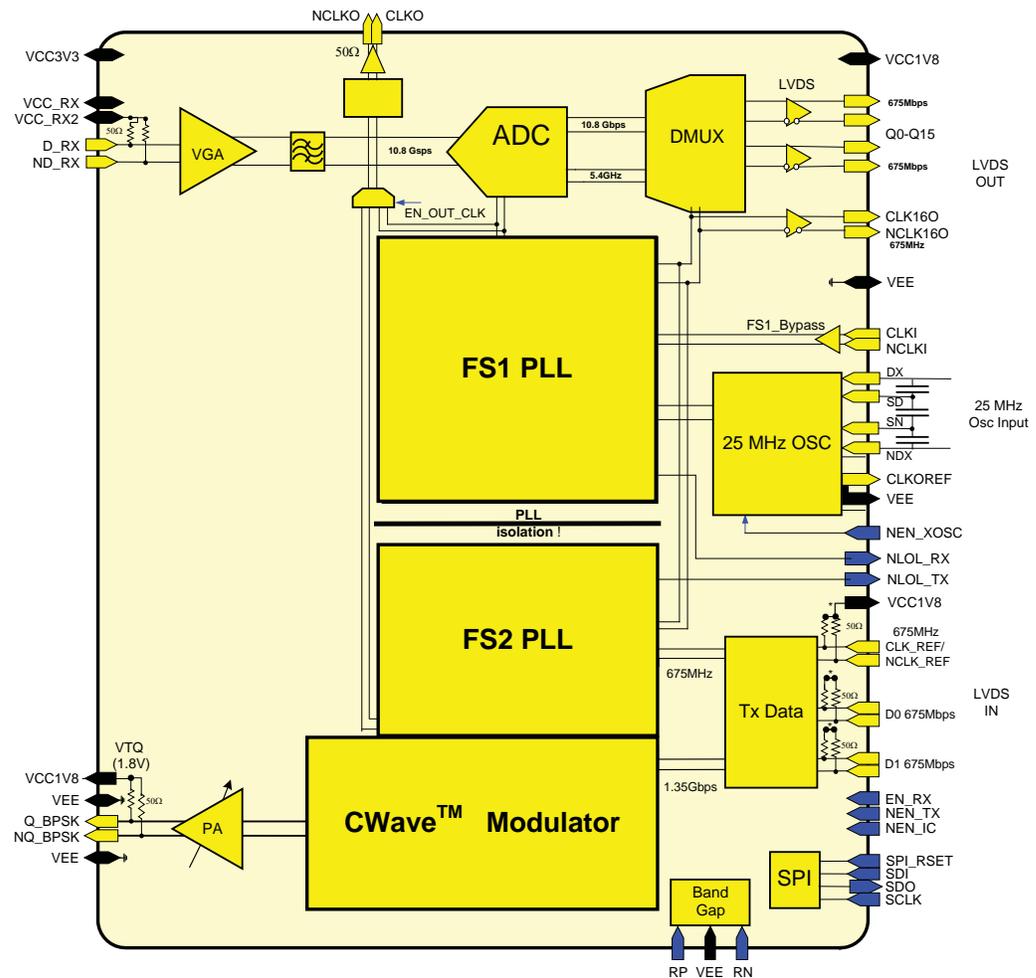


Figure 3: PL3120 Functional Block Diagram

Transmitter Block

CWave® Modulator/Transmitter

The transmitter (TX) block is based on the Pulse~Link CWave™ modulator. The BPSK modulator receives a 1.35 Gbps input data stream along with a 675 MHz ref-

reference clock from an external source via a two-bit on-chip MUX circuit. These two data bits are received synchronously using the 675 MHz reference clock from the PL3130 Baseband block. The basic function of frequency synthesizer FS2 is to act as a narrowband clock multiplier jitter filter for the input reference clock and to multiply the reference 675 MHz clock to synthesize a low-noise 4.05 GHz carrier clock. In addition, external CWave™ modulator clocking modes are implemented. The main blocks of the transmitter can be enabled/disabled by CMOS levels applied to the MUTE_TX pin with a switching time of less than 100 ns.

Output Differential Power Amplifier

The output Power Amplifier (PA) provides a variable-gain differential output power that is digitally controlled range from a 0 dBm to -213 dBm. On-chip 50-Ohm terminations are biased with an internal 1.8 V reference source. The transmit PA power control is provided through a 3-bit DAC controlled via the SPI interface. A typical plot of the PA *Output Power vs SPI* code is given in Figure 12. Refer to section 2.3.1 for an overview discussion on the Pulse~LINK SPI control bus.

8.1 GHz PLL Frequency Synthesizer

The clock required for retiming of incoming data is derived from the synthesized 4.05 GHz clock of the FS2 PLL. Retimed 1.35 Gbps low jitter data and the 4 GHz low noise clock are then used to produce the modulated CW output signal. The transmit FS2 PLL is an 8.1 GHz synthesizer that uses either an externally supplied 675 MHz reference from the PL3130 BBM interface, or using a 675 MHz reference supplied by the receiver's PLL frequency synthesizer FS1. A Lock detector is also provided to indicate proper functioning of the FS2 PLL.

Receiver Block

Variable Gain Amplifier Front-End

The input of the receiver block contains a digitally controlled 3-stage Variable Gain Amplifier (VGA). An on-chip 6-bit Digital-to-Analog Converter (DAC) with differential current output is used to control the VGA gain. Gain provided by each of the VGA stages can be regulated within a 2.5 dB to 17 dB range providing a maximum VGA gain of 50 dB and minimum gain of 7 dB. The differential D_RX/ND_RX input of the first stage integrates 50-Ohm terminations and requires external DC blocking capacitors. The second and third stages have on-chip AC coupled interconnections. The main blocks of the receiver (excluding FS1) can be enabled/disabled by CMOS levels applied to the NMUTE_RX pin with a switching time of less than 100 ns.

The receiver VGA gain is controlled via the SPI interface. Gain control is used by the PL3130 Baseband+MAC processes to optimize the receive channel performance. A typical plot of the VGA *Gain vs SPI* code is given in Figure 13.

ADC with Offset Control

The output of the variable gain amplifier stages is fed to an Analog-to-Digital Converter (ADC). The output of the ADC provides a data stream to the 16-channel De-

multiplexer (Demux). An SPI bus controlled 6-bit DAC also provides ADC offset control. The clock required for ADC sampling and Demux clocking is generated by PLL frequency synthesizer FS1 or can be sourced from an external reference clock source.

16-channel De-multiplexer

The 10.8 Gbps data stream is converted into sixteen pairs of 675 Mbps differential Demux data outputs along with a 675 MHz clock output (for synchronization purposes) for transferring the receive data to the PL3130 Baseband receiver inputs. The data and clock outputs of the receive data are standards-compliant Low Voltage Differential Signaling (LVDS) and require external 100 Ohm differential loads.

10.8 GHz PLL Frequency Synthesizer

PLL frequency synthesizer FS1 generates the required 10.8 GHz frequency used by the ADC and Demux circuits by multiplying its 25 MHz reference clock by a factor of 432. An external TCXO oscillator provides the 25MHz reference. An external 10.8 MHz reference clock may also be used to clock the ADC and is selected via the SPI interface. A Lock detector is also provided to indicate proper functioning of the FS1 PLL.

Control Interfaces

Transmit and receive functionality is primarily controlled through the SPI interface. The PL3120 Transceiver RFIC utilizes 8 SPI registers to interface with various internal blocks that are used to control operational settings, read processed data, and enable selection of input and output reference clocks. Internal PL3130 Baseband+MAC processes manage most of these control functions to optimize system performance and are not user accessible. Listed below are several of the functions that interface to the SPI registers.

- TX Modulator, TX/VGA power control, TX PLL/VCO
- RX/VGA, RX ADC, RX PLL/VCO
- Input reference clock selection and enables
- Output reference clock selection

Fast switching (100 ns) between transmit and receive modes is controlled by the dedicated control pins NMUTE_RX and MUTE_TX. A dedicated control pin NEN_IC also enables the shutdown of the PL3120 Transceiver RFIC.

SPI Control Interface

Four signal lines support the SPI Protocol defined in this specification, and are described below:

- SPI_RSET (SPI CYCLE RESET LOW) from SPI Master. SPI_RSET is normally low, and when low holds the RFIC SPI SLAVE logic in a reset condition and TRI-STATEs the SDO output. SPI_RSET is driven high during SPI write and read transactions. SPI_RSET has no effect on the SPI Slave's control register outputs.

- SCLK (SPI CLOCK) from SPI Master. The duty cycle of SCLK is 50%.
- SDI (SERIAL DATA IN) from SPI Master. MOSI=Master Out Slave In.
- SDO (SERIAL DATA OUT) to SPI Master. MISO=Master In Slave Out.

SPI Slave addressing is implemented in the SPI write and read transaction protocol, or frame structure. As such, there is no SPI chip select signal. The SPI protocol allows for a single SPI Master to talk to multiple ICs within a chipset, where each IC has an SPI Slave interface. Within this chipset SPI system, all SPI_RSET lines are connected together, all SCLK lines are connected together, all SDI (MOSI) lines are connected together, and all SDO (MISO) lines are connected together. Each control and status register pair must have a unique address. Across the chipset's SPI five bit address space, every control and status register pair must have a unique address. The five bit address field is common to all ICs in the chipset.

The three SPI input signals (SPI_RSET, SCLK, SDI) are compatible with 1.8V and 3.3V CMOS logic inputs. The SPI output signal (SDO) is a 3.3V CMOS TRI-STATE output. SDO is normally in a TRI-STATE condition, and is driven only during SPI read transactions. After the end of a read transaction, SDO returns to the TRI-STATE condition when SPI_RSET is driven low. Thus SDO TRI-STATE operation is automatic, and as such SPI writes to control SDO TRI-STATE operation are not needed. The maximum recommended SCLK frequency is 25 MHz.

An SPI transaction or frame consists of 24 bits for both write and read. There are exactly 24 SCLKs per transaction. SCLK remains low except during SPI transactions. There are 5 address bits, 1 R/W bit, 2 reserved bits, and 16 data bits in each transaction. The R/W bit indicates whether the transaction is a write or a read (R/W=0=write; R/W=1=read). The reserved bits are ignored by the slave. Write transactions contain 16 data bits sent from the SPI Master to the Slave. Read transactions contain 16 data bits sent from the SPI Slave to the Master. Details of write and read transactions are given in the following sections.

SPI Write Transaction

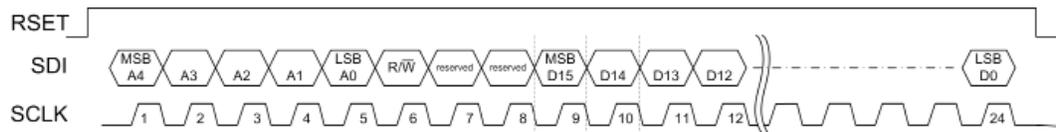


Figure 4: SPI Write Transaction

The SPI write transaction begins when the Master drives SPI_RSET high. Then about 1/2 the SCLK period later, the Master drives the first address bit A4 (MSB) onto SDI. After a setup interval of 1/2 the SCLK period, the Master issues the first SCLK rising edge. The Slave captures the information on SDI with the SCLK rising edge. The bit on SDI remains stable until the falling edge of SCLK, at

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which time the Master presents the next bit. After the 5 address bits are sent, the R/W bit (0=write) is sent. Next 2 reserved bits are sent. After the reserved bits, the Master sends the 16 data bits of the write transaction, starting with D15 and ending with D0. On the rising edge of the 24th SCLK, the SPI Slave whose address matches the SPI transaction address (A4 through A0) will load all 16 bits of the write transaction data into its 16 bit control output register. The Master drives SPI_RSET low 1 SCLK period after the rising edge of the 24th SCLK.

SPI Read Transaction

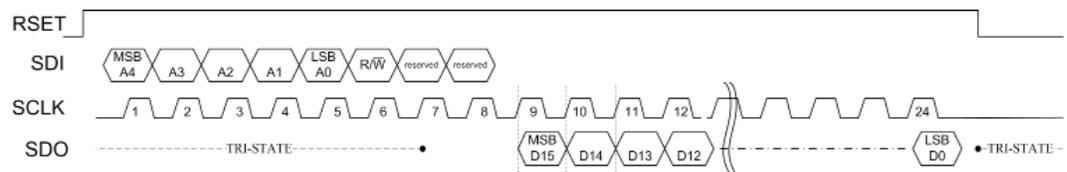


Figure 5: SPI Read Transaction

The SPI read transaction begins like the write transaction when the Master drives SPI_RSET high. Then about $\frac{1}{2}$ the SCLK period later, the Master drives the first address bit A4 (MSB) onto SDI. After a setup interval of $\frac{1}{2}$ the SCLK period, the Master issues the first SCLK rising edge. The Slave captures the information on SDI with the SCLK rising edge. The bit on SDI remains stable until the falling edge of SCLK, at which time the Master presents the next bit. After the 5 address bits are sent, the R/W bit (1=read) is sent. On the rising edge of the 7th SCLK, the SPI Slave whose address matches the SPI transaction address (A4 through A0) begins to drive SDO, taking SDO out of TRI-STATE. Also on the rising edge of the 7th SCLK, the SPI Slave captures or registers (not depicted in the figure) the 16 bits of read data that will be sent serially out SDO. Next the Master sends the 2 reserved bits on SDI. On the rising edge of the 9th SCLK, the addressed SPI Slave drives D15 (MSB of the read data) onto SDO. The Slave then sends D14 on the 10th rising edge of SCLK, and so forth, finishing with D0 on the 24th rising edge of SCLK. The Master captures or registers the SDO read data 1 SCLK period after the Slave launched the data (on the next rising edge of SCLK, or the equivalent time interval). The Master drives SPI_RSET low 1.5 SCLK periods after the rising edge of the 24th SCLK, and in response the SPI Slave TRI-STATES the SDO output.

Device Connections

Pad Configuration

The PL3120 Transceiver RFIC signal descriptions and pad assignments are described in this section. Shown in Figure 6 are the 12x12mm LGA package pad signal assignments.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	Test 4	Test 2	NMUTE_RX	NQ15	NQ14	NQ13	NQ12	NQ11	NQ10	NQ9	NQ8	NCLK160	VEE	VEE
B	Test 6	Test 3	Test 1	Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	CLK160	Q7	NQ7
C	VEEA_RX	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	Q6	NQ6
D	D_RX	VEEA_RX	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	Q5	NQ5
E	ND_RX	VEEA_RX	VEEA_RX	VCCA_RX2	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	Q4	NQ4
F	VEEA_RX	Test 5	VEEA_RX	VEEA_RX	VEEA_RX	VEE	VEE	VEE	VEE	VEE	VEE	VEE	Q3	NQ3
G	RSSI_AN	ADC_IN	VEE	VEE	VEE	VCCA_RX	VEE	VEE	VEE	VEE	VEE	VEE	Q2	NQ2
H	NCLKI	CLKI	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VCC1V8	VEE	VEE	Q1	NQ1
J	NCLKO	CLKO	VEE	VEE	VTQ	VEE	VEE	VEE	VEE	VCC3V3	VEE	VEE	Q0	NQ0
K	MUTE_TX	VEE	VEE	VEE	VCC1V8_2	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE
L	Q_BPSK	VEE	VEE	VEE	VEE	VEE	VCC3V3	VEE	VEE	VCC3V3D	VEE	VEE	NTUNE_RX	RETURN_RX
M	NQ_BPSK	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	NDX
N	VEE	VEE	VEE	VEE	VEE	VEE	RN	SDI	SCLK	NEN_XOSC	RETURN_TX	NL0L_RX	CLKOREF	SN
P	NDATA0	DATA0	NDATA1	DATA1	CLK_REF	NCLK_REF	RP	NEN_IC	SPL_RSET	SDO	NTUNE_TX	NL0L_TX	DX	SD

Figure 6: PL3120 12x12mm LGA Pad Configuration

Signal Description Summary

The following tables summarize the signal descriptions and pad connections for the PL3120 Transceiver RFIC chip.

Table 1: Type Designators

Type	Description
C	Control
DNC	Do Not Connect
G	Ground
P	Power
R	Reference

Table 2: Pad Descriptions

Name	Pad Num	Description	Additional Information	Type
VEEA_RX	C1, D2, E2-3, F1, 3-5	RX ground	Connect to GND	G

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Name	Pad Num	Description	Additional Information	Type
VCCA_RX2	E4	Positive power supply voltage for RX 2 nd VGA stage.	Connect to filtered +3.3V supply. Must be properly bypassed to RX ground with low ESR (effective series resistance) capacitor. Capacitors should be placed as close as possible to this pin.	P
D_RX	D1	Direct receiver (RX) RF input.	AC couple to 50 Ohm impedance input signal source	I
ND_RX	E1	Inverted receiver (RX) RF input.	AC couple to 50 Ohm impedance input signal source	I
TEST5	F2	Test Pin	Check of 11 bit of top SPI	DNC
VCCA_RX	G6	Positive supply voltage for RX 1 st VGA stage. Also termination for RF inputs.	Connect to filtered +3.3V supply. Must be properly bypassed to RX ground with low ESR capacitor. Capacitors should be placed as close as possible to this pin.	P
Reserved	G1	Test pin	Test for RSSI	DNC
Reserved	G2	Test Input to 8 Bit RSSI ADC	Apply voltage to this pin to test 8 Bit ADC, a value can be read by SPI.	DNC
VEE	A13, 14, C2-12, D3-12, E5-12, F6-12, G3-5, 7-12 H3-9 11,12 J3,4,6-9, 11,12, K2-4, 6-14 L2-6, 8, 9,11,12 M2-13, P1-6	Ground	Connect to GND	G
CLKI	H2	Direct external clock signal bypassing ASIC internal frequency synthesizer FS1.	Leave open if not used (regular operation). If used, AC couple to 50 Ohm impedance clock signal source.	I
NCLKI	H1	Inverted external clock signal bypassing ASIC internal frequency synthesizer FS1.	Leave open if not used (regular operation). If used, AC couple to ground through 50 Ohm.	I
CLKO	J2	Direct /8, /4, /2, /1 clock output from FS1 or FS2	AC couple to 50 Ohm impedance load	O

Name	Pad Num	Description	Additional Information	Type
NCLKO	J1	Inverted /8, /4, /2, /1 clock output from FS1 or FS2	AC couple to 50 Ohm impedance load	O
MUTE_TX	K1	BPSK data output ON/OFF. NMOS input.	Leave open or connect to ground to enable transmitter. Connect to +1.8/2.5/3.3V (see V_{III} description) to mute.	C
VTQ	J5	Termination voltage for TX RF outputs.	Connect to filtered +1.8V supply. Must be properly bypassed to ground with low ESR capacitor. Capacitors should be placed as close as possible to this pin.	P
Q_BPSK	L1	Direct transmitter (TX) RF output	AC couple to 50 Ohm impedance load	O
NQ_BPSK	M1	Inverted transmitter (TX) RF output	AC couple to 50 Ohm impedance load	O
VCC1V8_2	K5	+1.8V Power supply input.	Connect to filtered +1.8V supply. Must be properly bypassed to ground with low ESR capacitor. Capacitors should be placed as close as possible to this pin.	P
NDATA0	P1	Inverted BPSK modulator input data Bit 0.	LVDS standard signaling.	I
DATA0	P2	Direct BPSK modulator input data Bit 0	LVDS standard signaling.	I
NDATA1	P3	Inverted BPSK modulator input data Bit 1.	LVDS standard signaling.	I
DATA1	P4	Direct BPSK modulator input data Bit 1.	LVDS standard signaling.	I
CLK_REF	P5	Direct 675MHz 50 Ohm impedance reference clock input.	LVDS standard signaling.	I
NCLK_REF	P6	Inverted 675MHz 50 Ohm impedance reference clock input	LVDS standard signaling.	I
RP	P7	External reference resistor for generating PTAT voltage.	Connect 918.4Ohm resistor between RP and VEE pin.	R
RN	N7	External reference resistor for generating NTC voltage.	Connect 30KOhm resistor between RN and VEE pin.	R
NEN_IC	P8	Master transceiver enable/disable control. Capacitance is 0.4pF.	Leave open or connect to ground to enable transceiver. Connect to +1.8/2.5/3.3V to disable.	C

Name	Pad Num	Description	Additional Information	Type
VCC3V3	L7, J10	+3.3V Power supply input.	Connect to filtered +3.3V supply. Must be properly bypassed to ground with low ESR (effective series resistance) capacitor. Capacitors should be placed as close as possible to this pin.	P
SDI	N8	SPI serial data input.	3.3V CMOS signal levels. Refer to SPI description.	I
SPI_RESET	P9	SPI RESET	3.3 V CMOS signal. Low level for SPI slave logic reset. Has no effect on the slave's control register outputs. High level during SPI Read / Write Transactions.	I
SCLK	N9	SPI serial clock input.	3.3V CMOS signal levels. Refer to SPI description.	I
SDO	P10	SPI serial data output	3.3V CMOS signal levels. Refer to SPI description.	O
NEN_XOSC	N10	On-chip crystal oscillator enable control. Independent from chip enable NEN_IC input.	Connect to ground to enable crystal oscillator (normal operation). Connect to +1.8/2.5/3.3V (see V _{IH} description to disable).	C
NTUNE_TX	P11	Output for the integration capacitor of the FS2 PLL.	Connect capacitor between NTUNE_TX and RETURN_TX.	O
RETURN_TX	N11	Return path for NTUNE_TX integration capacitor.	Connect capacitor between NTUNE_TX and RETURN_TX.	I
NLOL_TX	P12	FS2 PLL loss of lock indicator. Lock condition indicated when NLOL = HIGH. Loss of lock condition indicated when NLOL=LOW. The indicator bit is also available through SPI.	3.3V CMOS logical levels. See application schematic for LED indication of LOL. For test purposes NLOL can be pulled down to -5V through 10KOhm resistor. Phase detector and OTA will be disabled and NTUNE pin can be used to control VCO frequency (for test purposes only).	O

Name	Pad Num	Description	Additional Information	Type
NLOL_RX	N12	FS1 PLL loss of lock indicator. Lock condition indicated when NLOL = HIGH. Loss of lock condition indicated when NLOL = LOW. The indicator bit is also available through SPI.	3.3V CMOS logical levels. See application schematic for LED indication of LOL. For test purposes NLOL can be pulled down to -5V through 10KOhm resistor. Phase detector and OTA will be disabled and NTUNE pin can be used to control VCO frequency (for test purposes only).	O
VCC3V3D	L10	+3.3V Digital Power supply input.	Connect to filtered +3.3V supply. Must be properly bypassed to ground with low ESR (effective series resistance) capacitor. Capacitors should be placed as close as possible to this pin.	P
CLKOREF	N13	25MHz reference clock output from crystal oscillator.	3.3V CMOS output. Driving capability is 20pF.	O
VEED	M13	Ground	Connect to GND	G
DX	P13	Direct input for external 25MHz crystal or VCXO.	Connect crystal or AC couple one of the outputs of differential clock source. Use as short as possible trace on board.	I
SD	P14	External Cap for XTAL Resonator	Place a 48pF(1%) Cap between SD and DX. A 24pF(1%) cap shall be connected between SD and SN.	I
SN	N14	External Cap for XTAL Resonator	Place a 48pF(1%) Cap between SN and NDX. A 24pF(1%) cap shall be connected between SD and SN.	I
NDX	M14	Inverted input for external 25MHz crystal or VCXO.	Connect crystal or AC couple one of the outputs of differential clock source. Use as short as possible trace on board.	I
NTUNE_RX	L13	Input for the integration capacitor of the FS2 PLL.	Connect capacitor between NTUNE_RX and RETURN_RX.	O
RETURN_RX	L14	Return path for NTUNE_RX integration capacitor.	Connect capacitor between NTUNE_RX and RETURN_RX.	I

Name	Pad Num	Description	Additional Information	Type
VCC1V8	H10	+1.8V Power supply input.	Connect to filtered +1.8V supply. Must be properly bypassed to ground with low ESR capacitor. Capacitors should be placed as close as possible to this pin.	P
NQ0	J14	Inverted Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q0	J13	Direct Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ1	H14	Inverted Q1 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q1	H13	Direct Q1 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ2	G14	Inverted Q2 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q2	G13	Direct Q2 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ3	F14	Inverted Q3 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q3	F13	Direct Q3 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ4	E14	Inverted Q4 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q4	E13	Direct Q4 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ5	D14	Inverted Q5 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q5	D13	Direct Q5 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ6	C14	Inverted Q6 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q6	C13	Direct Q6 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ7	B14	Inverted Q7 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O

Name	Pad Num	Description	Additional Information	Type
Q7	B13	Direct Q7 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
CLK16O	B12	Direct C/16 clock output. Delay matched with Q0...Q15 outputs.	Connect to LVDS compatible input. Clock frequency is 675MHz. 1.2V common mode voltage.	O
NCLK16O	A12	Inverted C/16 clock output. Delay matched with Q0...Q15 outputs.	Connect to LVDS compatible input. Clock frequency is 675MHz. 1.2V common mode voltage.	O
NQ8	A11	Inverted Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q8	B11	Direct Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ9	A10	Inverted Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q9	B10	Direct Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ10	A9	Inverted Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q10	B9	Direct Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ11	A8	Inverted Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q11	B8	Direct Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ12	A7	Inverted Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q12	B7	Direct Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ13	A6	Inverted Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q13	B6	Direct Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ14	A5	Inverted Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O

Name	Pad Num	Description	Additional Information	Type
Q14	B5	Direct Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NQ15	A4	Inverted Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
Q15	B4	Direct Q0 DMUX output.	Connect to LVDS compatible input. Data rate is at 675Mb/s. 1.2V common mode voltage.	O
NMUTE_RX	A3	Receiver fast enable (100ns). NMOS input.	Leave open or connect to ground to mute. Connect to +1.8/2.5/3.3V (see V_{IH} description) to enable data out. Fast rise/fall is required. Capacitance on the pin is 0.5pF.	C
TEST1	B3	Reserved	SPI PON RESET Test	DNC
TEST2	A2	Reserved	ESD test	DNC
TEST3	B2	Reserved	VGA DAC Current Control	DNC
TEST4	A1	Reserved	VGA Current Control Replica	DNC
TEST6	B1	Reserved	ESD test	DNC

Electrical Specifications

Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Description	Symbol	Min	Max	Units
Power supplies voltages.	VCC1V8	-0.5	+3.5	V
	VCC3V3	-0.5	+5	V
RX RF inputs (D_RX , ND_RX) voltage.		-0.5	+5	V
TX RF inputs ($DATA$, NDA , CLK_REF , $NCLK_REF$, CLK_EXT4G , $NCLK_EXT4G$) voltage.		-0.5	+3.5	V
CMOS control input voltage.		-0.5	+3.5	V
Junction Temperature.	T_j	-25	+125	°C

Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Description	Value
Relative Humidity	95%
Ambient Operating Temperature	0 C to +70 C

DC Characteristics

Table 5: DC Electrical Characteristics

Parameters		Conditions	Min	Typ	Max	Units
Power supply.						
3.3V supply voltage V_{CC3V3} .			3.1	3.3	3.5	V
1.8V supply voltage V_{CC1V8} .			1.7	1.8	1.9	V
Shutdown mode supply current.	1.8V supply	Rx-OFF, Tx-OFF, PLL Rx-OFF, PLL Tx-OFF, ADC_8bit-OFF, Refs-OFF		8		mA
	3.3V supply			15		
Standby mode supply current.	1.8V supply	Rx-OFF, Tx-OFF, PLL Rx-OFF, PLL Tx-OFF, ADC_8bit-OFF		12		mA
	3.3V supply			73		
Receive mode supply current.	1.8V supply	T=125°C, NEN_IC=V _{IL} , MUTE_TX=V _{IH} , NMUTE_ RX=V _{IH}	74	83	88	mA
	3.3V supply		176	192	216	
Transmit mode supply current.	1.8V supply	T=125°C, NEN_IC=V _{IL} , MUTE_TX=V _{IL} , NMUTE_ RX=V _{IL}	112	119	133	mA
	3.3V supply		130	146	163	
Total (Tx/Rx mode) supply current.	1.8V supply	T=125°C, NEN_IC=V _{IL} , MUTE_TX=V _{IL} , NMUTE_ RX=V _{IH}	159	172	186	mA
	3.3V supply		177	194	218	
Control Logic I/O						
Digital input voltage high (V _{IH}).			1.7		3.5	V
3V3 CMOS input voltage high (V _{IH3V3}).			VCC3V3-0.5			V
Digital input voltage low (V _{IL}).					+0.5	V
Digital output voltage high (V _{OH}).		NLOL output current sinking/ sourcing 20mA.	VCC3V3-0.5			V
Digital output voltage low (V _{OL}).					+0.5	V

Parameters	Conditions	Min	Typ	Max	Units
RX backend DMUX LVDS data and clock outputs (Q0...Q15, NQ0...NQ15, CLK16O, NCLK16O).					
Output single-ended swing (V_{OUT_LVDS}).	Outputs differentially terminated with $R_T=100$ Ohm.	250	350	450	mV
Output differential swing (V_{DOUT_LVDS}).		500	700	900	mV
Output voltage high (V_{OH_LVDS}).				1.5	V
Output voltage low (V_{OL_LVDS}).		0.9			V
Output common mode (V_{OCM_LVDS}).		1.125	1.2	1.275	V
TX differential LVDS inputs (DATA0, NDATA0, DATA 1, NDATA1 CLK_REF, NCLK_REF).					
Input single-ended voltage swing (V_{IN_TX}).		125	200	400	mV
Input differential swing (V_{DIN_TX}).		250	400	800	mV
Input common mode (V_{CM_TX}).		0.4	1.2	2.0	V
Input termination.			100		Ohm

AC Electrical Characteristics

Receiver Block

Table 6: Receiver AC Electrical Characteristics

Parameters	Conditions	Min	Typ	Max	Units
RF frequency range (F_{IN}).	$V_{CC}=3.15V$ to $3.5V$	3.0	4.0	5.0	GHz
ADC sampling frequency (F_S).	$V_{CC}=3.15V$ to $3.5V$		10.8	12	GHz
Maximum VGA gain (G_{MAX}).	Controlled by $RX_GC<0...7>$ bits. See Figure 13.		50		dB
Minimum VGA gain (G_{MIN}).			7		dB
Input referred IP3 (IIP3).	Gain= G_{MAX}		-34		dBm
	Gain= G_{MIN}		-3		
Input return loss (S11).				-11	dB
1dB compression point (1dB _{CP}).	Gain= G_{MAX}		-43		dBm
	Gain= G_{MIN}		-4		
Noise figure (NF).	Gain= G_{MAX}		9		dB
	Gain= G_{MIN}		18		dB

Parameters	Conditions	Min	Typ	Max	Units
ADC sensitivity (V_{IN_MIN}).	$F_S = 10.8\text{GHz}$, $F_{IN} = 4\text{GHz}$		10		mVp-p
Switching time (T_{on}).	Standby to receive mode.			100	ns
Control DAC settling time (T_{SETTLE}).				1	us
DMUX data outputs ($Q0-Q15$) bitrate.			675	750	Mbps
DMUX clock $CLK160$ output frequency.			675	750	MHz
*Maximum absolute skew between data $Q0-Q15$ and $CLK160$ outputs (t_{SKEW}).	Over corners, junction temperature $T_j = [-25 \dots 125]^\circ\text{C}$ and power supply @ 675MHz. See Figure 9	-200		290	ps
DMUX clock $CLK160$ output rise/fall time	Signal levels 20/80			120	ps
DMUX clock $CLK160$ output duty cycle		45	50	55	%

*Data could switch before and after the rising clock edge

Transmitter Block

Table 7: Transmitter AC Electrical Characteristics

Parameters	Conditions	Min	Type	Max	Units
Output bit rate.			1.35		Gbps
Input carrier frequency.			4.05		GHz
Minimum output peak power level.	On 50 Ohm impedance load			-21	dBm
Maximum output peak power level.		0			dBm
Output return loss (S22).				-10	dB
Switching time (T_{SWITCH}).	Standby to transmit mode.			100	ns

PLL Frequency Synthesizer

Table 8: PLL Frequency Synthesizer AC Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Lock Acquisition Time (T_{LOCK}).	F_{in} step=10MHz	47	500	1000	us
Output Clock Duty Cycle (DC).			50	53	%
Phase Noise (σ_f).	@1MHz offset		-95		dBc/Hz

Control & Support Interface Timing

As previously shown in the PL3120 functional interface diagram in Figure 1, there are data, control and support interfaces to the PL3130 Baseband+MAC chip. Each of these interfaces have specific data format and timing requirements associated with them as detailed in the following sections.

RF SPI Timing

SPI interface timing is shown in Figure 7 for both write and read transactions. On a write transaction (including the address bits, R/W, and reserved bits for both write and read transactions), SDI is stable approximately $\frac{1}{2}$ SCLK period before, and through to $\frac{1}{2}$ SCLK period after the SCLK rising edge the Slave uses to capture or register the SDI write data. On a read transaction, SDO is launched by the Slave on an SCLK rising edge and captured or registered by the Master on the next SCLK rising edge. Thus SDO has 1 SCLK period to become valid before being captured by the Master.

Table 9: RF SPI Timing

Constraints relative to rising edge of SCLK (at 12.5MHz) are:

Signal	Parameter	Min	Max	Units	Notes
SDI	Setup	4		ns	
	Hold	4		ns	
SDO	Output Valid	0	8	ns	

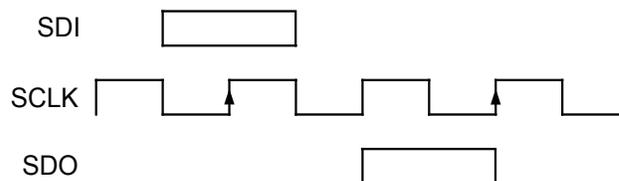


Figure 7: SPI Read and Write Timing Diagram

Figure 8 depicts the SPI Reset timing for both write and read transactions. The transaction begins when the Master drives SPI_RSET high. Then about $\frac{1}{2}$ the SCLK period later, the Master drives the first address bit A4 (MSB) onto SDI. After a setup interval of $\frac{1}{2}$ the SCLK period, the Master issues the first SCLK rising edge. SPI Reset timing at the end of a read transaction where the Master drives SPI_RSET low 1.5 SCLK periods after the rising edge of the 24th SCLK is shown. Not depicted is the case of SPI Reset timing occurring at the end of a write transaction where the Master drives SPI_RSET low 1 SCLK period after the rising edge of the 24th SCLK.

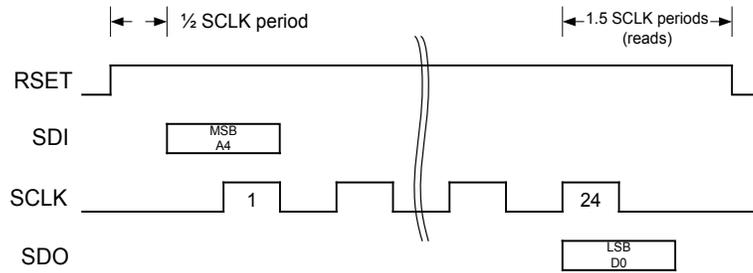


Figure 8: SPI Reset Timing Diagram

RX Output Data Timing

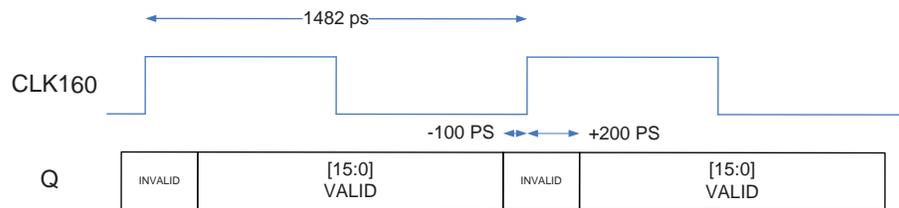


Figure 9: Rx Clock & Data Timing

TX Input Data Timing

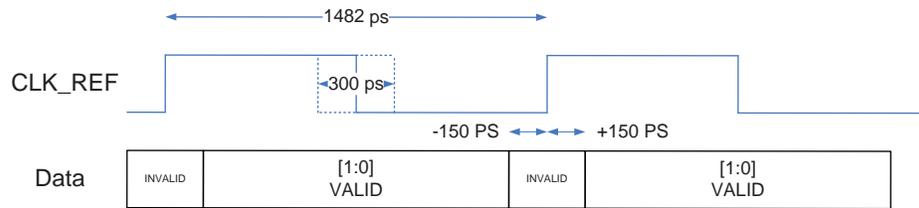


Figure 10: Tx Clock & Data Timing

Operation Modes Switching Timing

The internally controlled switching of operation modes has delays associated with recharging of parasitic capacitances, PLLs and VCOs startup times. Delay between applying of appropriate signal (NEN_IC, NEN_XOSC, NMUTE_RX and MUTE_TX) and operational mode change is shown in Figure 10.

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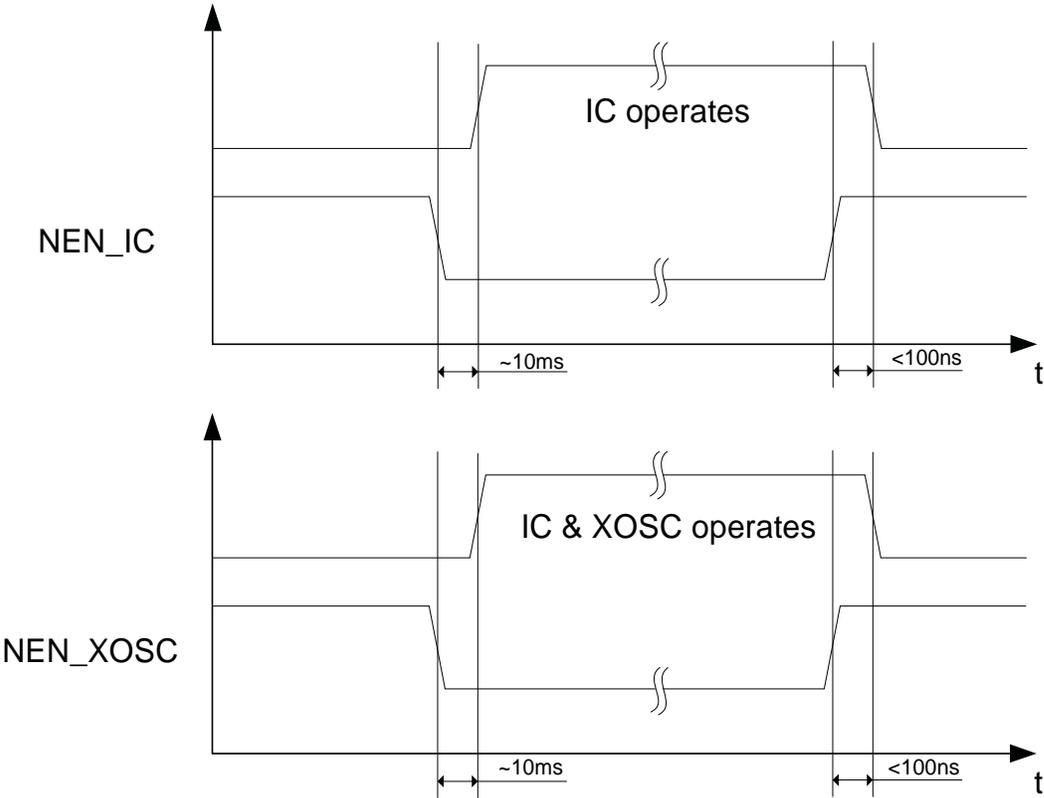


Figure 11: Operation Modes Switching Timing

Typical Operating Characteristics

Modulator Peak Output Power vs Control Code

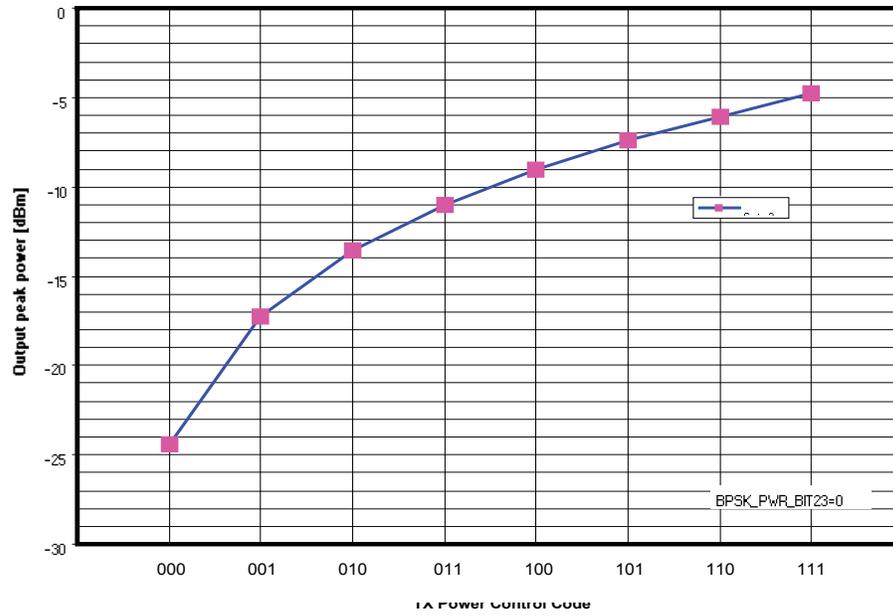


Figure 13: Modulator Peak Output Power vs Control Code

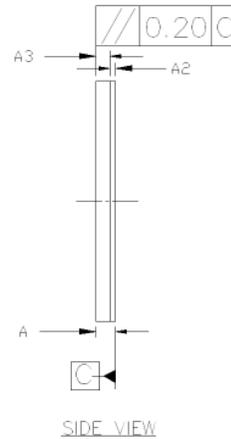
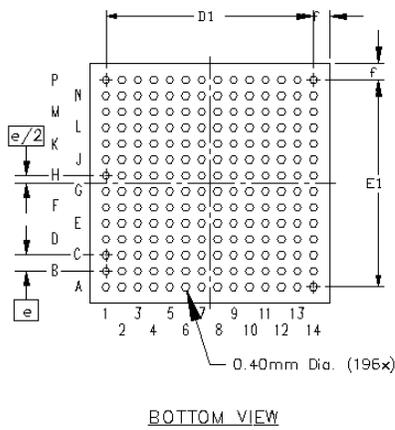
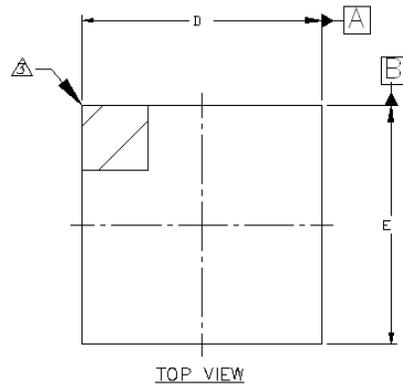
Mechanical Specifications

Table 10: PL3120 Transceiver RFIC Mechanical Specifications

Area	Dimensions
Compliance	Per JEDEC MO-216
Size	12 x 12 mm
Connection Points	196 Pads
Pad Pitch	0.80 mm BSC
Nominal Thickness	.96 mm

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SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.87	0.96	1.05	.034	.038	.041
A1	-	-	-	-	-	-
A2	0.22	0.26	0.30	.009	.010	.012
A3	0.65	0.70	0.75	.026	.028	.030
b	-	-	-	-	-	-
D	11.90	12.00	12.10	.469	.472	.476
D1	10.40 BSC			.409 BSC		
E	11.90	12.00	12.10	.469	.472	.476
E1	10.40 BSC			.409 BSC		
e	0.80 BSC			.031 BSC		
f	0.70	0.80	0.90	.028	.031	.035



- NOTES :
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M - 1994.
 2. CONTROLLING DIMENSIONS ARE IN MM.
 3. DETAILS OF A1 CORNER ARE OPTIONAL, AND MAY CONSIST OF INK DOT, LASER MARK OR METALIZED MARKING, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
 4. REFER TO JEDEC OUTLINE MO-216 FOR DATUMS, FEATURES AND DIMENSIONS NOT SHOWN.

Figure 14: 196-pad LGA Package Dimensions

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Acronyms & Abbreviations

ASIC	Application Specific Integrated Circuit
BB	Baseband
DEV	802.15.3 Device
EVK	Evaluation Kit
LNA	Low Noise Amplifier
lsb	Least Significant Bit
LSB	Least Significant Byte
MAC	Media Access Control
msb	Most Significant Bit
MSB	Most Significant Byte
OB	Output Buffer
PHY	Physical Layer
PLL	Phase Lock Loop
PNC	802.15.3 Piconet Coordinator
TDMA	Time Division Multiple Access
UWB	Ultra-Wideband
VGA	Variable Gain Amplifier

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