Pulse~LINK®

PL3100 CWave®Chipset

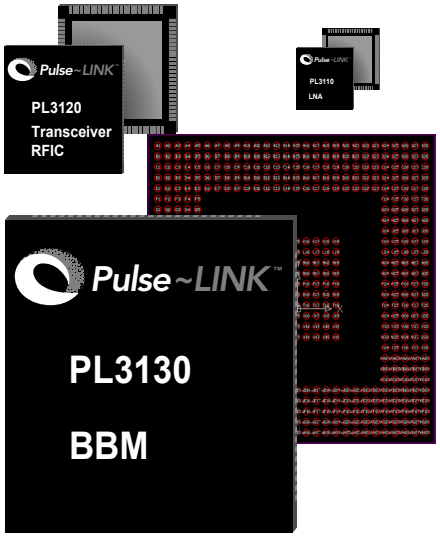
OVERVIEW

Pulse-LINK's PL3100 CWave™ chipset is designed for isochronous wireless or wired communication networks. With data rates up to 1012 Mbps, the chipset is particularly suited to supporting triple play services over coaxial cable. The PL3100 operates in the 3.1-4.7 GHz frequency range, allowing coexistence with DOCSIS, analog or digital cable television channels, MoCA and satellite

The PL3100 chipset comprises three integrated circuits:

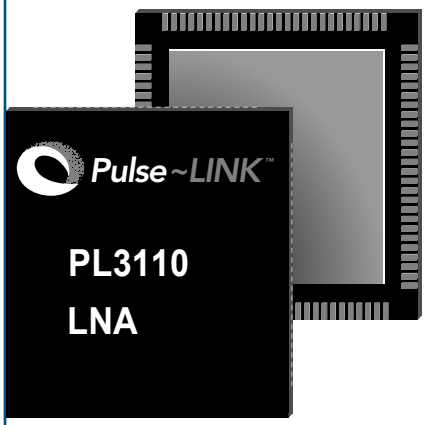
- The PL3110 low noise wideband RF amplifier (LNA)
- The PL3120 RFIC transceiver front end
- The PL3130 combined digital Baseband and MAC (802.15.3 compliant)

It uses a PCI interface to accept or output content and for system control. For convenience, the PL3100 also provides eight general purpose I/O pins that may be used to detect external events or control external devices.



PL3110 Ultra-Wideband LNA

The PL3110 is a low noise ultra wideband amplifier which connects to an antenna. It amplifies two RF receive channels, operating over a wide frequency range from 3.1-5.8 GHz, optimized at the center frequency of 4 GHz. It includes:



- A control interface to set the modes of operation such as bypass mode of LNAs, enable/disable mode, and gain control for two Low Noise wideband Amplifiers (LNA)
- Two double stages of Variable Gain Amplifiers (VGA)
- Two independent LNAs to enable RX diversity
- An output amplifier

It has a 2.5dB typical noise figure at 4 GHz and 2dBm input third order intercept point (IP3). Maximum gain is 45dB; minimum gain is 10dB. This can operate in a single channel mode or combined two channel mode. This is packaged in a 40 lead QFN package.

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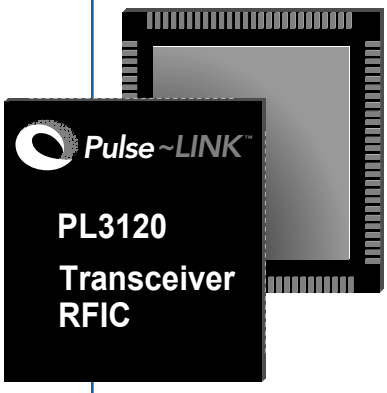
LNA Characteristics

Parameter		Value			Units	Notes
		min	nom	max		
Power supply voltage	Vcc	3.15	3.3	3.5	V	3.3V nominal
Frequency range	BW	3.1	4.46	5.82	GHz	-3dB point
Noise Figure	NF			2.5	dB	
Voltage gain	Kv	10		45	dB	
Input dynamic range	P1dB	-100		-10	dBm	
Power Supply Rejection Ratio	PSRR	60		dB		200mV p-p SE at 50 Ohms
Common Mode Rejection Ratio	CMRR	60		dB		
Architecture						Fully differential

PL3120 RFIC Front End

The PL3120 comprises independent transmitter and receiver sections. The transmitter serializes data from the PL3130, generates the 4 GHz carrier, modulates the carrier with the serialized data, and filters the output, which can drive an antenna directly in typical UWB applications. The receiver section receives pre-amplified incoming RF data, demodulates it, and oversamples it with a high-speed A/D converter.

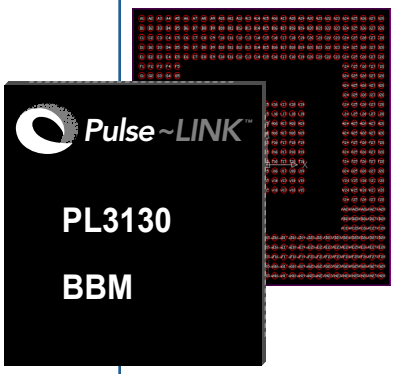


The resulting incoming digital data stream is then demultiplexed for connection with the PL3130. The PL3130 sets the PL3120's RF amplifier gain and reads its received signal strength indication (RSSI) over a dedicated 3-wire serial bus. It also includes frequency synthesizers (FS1, FS2 and OSC), and control interface. Digitally controlled TX/RX/standby/sleep modes allow minimization of power consumption by fast (<100ns) switching of TX and RX ASIC circuitry. Receiver amplifier chain contains digitally controlled 3-stage variable gain amplifier (VGA) also. An on-chip 8-bit digital to analog converter (DAC) with differential current output is used to control VGA gain within 7dB to 50dB range. VGA output signal is fed to 10.8 G s/s 1-bit ADC, the digital output of which is deserialized in 1:16 DEMUX for later processing in baseband chip. 16 pairs of 675 Mbps LVDS compliant data outputs along with 1.35 GHz clock output (for synchronization purposes) are provided for transfering the data to baseband ASIC.

Modulator output peak power is digitally controlled within –21dBm to 0dBm range for each output. Combined outputs deliver –18 to +3dBm. The CWave® modulator receives 1.35 Gbps input data along with 1.35 GHz reference clock from the baseband ASIC PL3130. The PL3120's functions and parameters are controlled either through the SPI serial interface or dedicated pins. Integrated 8-bit successive approximation ADC with SPI interface is used for RSSI and ASIC temperature readout. The PL3120 operates from +3.3V and +1.8V power supplies and is specified for operation from –40°C to +90°C. It is available in a 104 pin QFN package.

PL3130 Baseband + MAC

The PL3130 connects directly to the host system via a standard 32-bit PCI bus. In a typical system it also connects directly to an external SD-RAM and to the PL3120, and includes a serial interface. It requires a 1.35 GHz clock, which is provided by the PL3120, as well as the PCI bus clock.



The PL3130's functions in a UWB communication system include:

- Encode and modulate data for transmission over the UWB channel
- Decode and demodulate data for reception from the channel
- Apply forward error correction (FEC) coding and decoding
- Apply data whitening/scrambling
- Generate and recover synchronization signals
- Receive control signals from the host
- Forward appropriate control signals to the PL3120
- Receive status signals from the PL3120.

The PL3120 always modulates the CWave® carrier at a nominal rate of 1.35 G chips/second, but supports five different effective data rates, summarized in the table below:

chips/bit	data rate (Mb/s)
1.35	1012
2	675
8	169
16	84
64	21

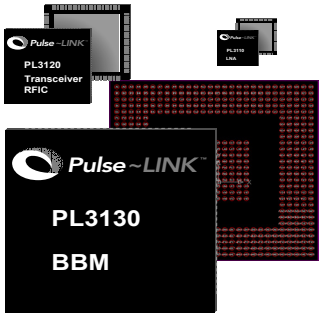
As in any communication system, the user must select a data rate which optimzes the inherent tradeoffs among link range, application error tolerance, application throughput requirements, and ambient interference.

PL3100 Chipset

Designed for high data-rate wired or wireless applications, the PL3100 offers new possibilities for short-range wireless communications, long-range point-to-point microwave and robust networking over copper twisted-pair and coaxial cable.

The PL3100 provides the advanced error correction techniques of Pulse~LINK's patented CWave® technology. Able to assemble into ad-hoc networks of up to 16 nodes, the PL3130 uses a 802.15.3 Time Division Multiple Access (TDMA) MAC layer to insure that each receiver is guaranteed the necessary bandwidth for low-latency services such as video and voice.

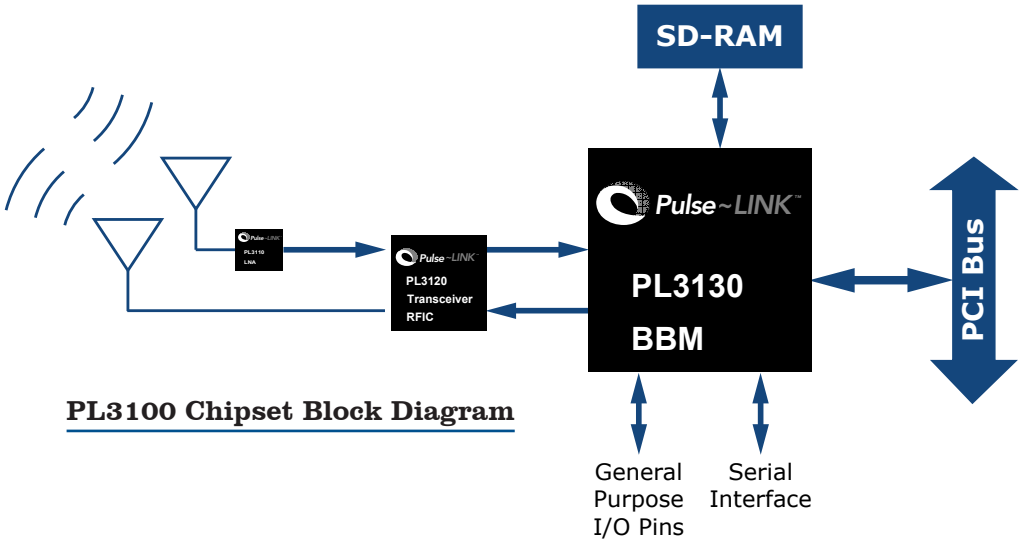
A typical use-case for the CWave® PL3100 is to provide Triple Play services to Homes or MDUs (Multi Dwelling Units). MSOs such as Cable, Satellite and Telcos (FTTH) need to extend coverage from Point of Entry (PoE) to multiple rooms or offices. Most homes and apartment buildings can leverage existing Cable TV wiring by using CWave® to delivery voice, video and data to any room with a TV wall outlet.



Other use-cases include: Extending digital services into schools, hotels and medical facilities, upgrading analog video surveillance systems to digital, Point-to-Point Microwave, In-Vehicle communication and entertainment systems and Military and Avionics applications.

Physical Characteristics

PHY Rate: up to 1012 Mbps.	**Power supplies: 3.3V, 2.5V, 1.2V.**
Range: up to 12 meters at 84 Mbps.	**Operating temperature range: 0-70 degrees C.**
Interfaces: 32-bit wide PCI 2.1, 8 General Purpose I/O (GPIO) pins.	**PL3110 – 40 pin QFN. PL3120 – 104 pin QFN. PL3130 – 560 pin PBGA.**



PL3100 Chipset Block Diagram

Feature Summary

- Mixerless transmitter architecture without digital to analog conversion (DAC)
- Mixerless coherent receiver with improved dynamic range
- FEC (Forward Error Correction) and multipath mitigation methods LDPC (Low Density Parity Codes) and MISO (Multiple-Input Single Output) Equalizer
- Fast synchronization acquisition and open-loop architecture
- Link adaptation for optimum performance and quality
- Point-to-multipoint support
- Support for traffic classes with QoS constraints.

ORDERING INFORMATION

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PL3100	**CWave® Chipset**

About Pulse~LINK

Pulse~LINK, Inc. is a fabless semiconductor company with more than 300 issued and pending telecommunication patents. Headquartered in Carlsbad, California, Pulse~LINK is the inventor of CWave®, an innovative, simple digital RF architecture enabling high data-rate home networking over coax.